We Claim:

1. A circuit configuration, comprising:

a first amplifier having a first controlled path connected to ground and a first terminal for receiving a signal to be amplified;

a second amplifier having a second controlled path connected to ground and a second terminal for receiving a signal to be amplified; and

a switching element having a switched path with a first side connected to ground and with a second side connected to one of said first and second terminals, said switched path of said switching element being configured to be controllable by a signal present at another one of said first and second terminals.

2. The circuit configuration according to claim 1, wherein said second amplifier is configured to be operated in dependence on one of a voltage level and a voltage profile established at said first terminal of said first amplifier.

3. The circuit configuration according to claim 1, wherein:

said first and second amplifiers are configured to amplify analog AC voltages; and

said second amplifier is configured to be operated in dependence on a DC voltage level established at said first terminal of said first amplifier.

4. The circuit configuration according to claim 3, wherein said first and second amplifiers are configured such that a DC voltage established at said second terminal of said second amplifier is varied depending on the DC voltage level established at said first terminal of said first amplifier.

5. The circuit configuration according to claim 1, including a DC voltage generating circuit connected to said first terminal of said first amplifier and to said second terminal of said second amplifier for providing DC voltages to said first and second terminals.

6. The circuit configuration according to claim 5, wherein said DC voltage generating circuit generates the DC voltages with given values such that said first and second amplifiers are enabled to amplify signals to be amplified.

7. The circuit configuration according to claim 3, wherein said first and second amplifiers are configured such that, if

a DC voltage established at said first terminal of said first amplifier has a given value at which signals to be amplified by said first amplifier can be amplified, then a DC voltage established at said second terminal of said second amplifier is left at or brought to a value at which the second amplifier is unable to amplify signals to be amplified.

8. The circuit configuration according to claim 3, wherein said first and second amplifiers are configured such that, if a DC voltage established at said first terminal of said first amplifier has a given value at which said first amplifier is unable to amplify signals to be amplified, then a DC voltage established at said second terminal of said second amplifier is left at or brought to a value at which said second amplifier is able to amplify signals to be amplified.

9. The circuit configuration according to claim 3, wherein said first amplifier is configured such that a DC voltage established at said first terminal of said first amplifier is one of adjustable and variable via said first terminal for receiving signals to be amplified by said first amplifier.

10. The circuit configuration according to claim 1, wherein:

said first amplifier is a first transistor and said second amplifiers is a second transistor; and

said first amplifier has a gate terminal, said second transistor is configured to be operated in dependence of one of a voltage level and a voltage profile established at said gate terminal of said first transistor.

11. The circuit configuration according to claim 1, wherein:

said first amplifier is a first transistor and said second amplifiers is a second transistor;

each of said first and second transistors has a first gate terminal, a second gate terminal and a controlled path;

said first gate terminal of said first transistor forms said first terminal for receiving a signal to be amplified, said first gate terminal of said second transistor forms said second terminal for receiving a signal to be amplified;

said second gate terminal is a terminal for setting a gain;

further transistors are respectively assigned to said first and second amplifiers;

each of said further transistors has a controlled path and two gate terminals;

said first and second gate terminals of said first and second transistors are coupled to respective ones of said two gate terminals of said further transistors; and

said controlled path of each of said further transistors is connected to ground and coupled to said controlled path of a respectively assigned one of said first and second amplifiers.

12. The circuit configuration according to claim 11, including:

two series circuits, each of said series circuits including two resistors and a node between said two resistors;

said first and second terminals of said first and second amplifiers being coupled to respective ones of said two gate terminals of said further transistors via said two series circuits; and

said switching element having a control terminal, said switched path of said switching element and said control terminal of said switching element being respectively coupled to said node of a respective one of said two series circuits.